# UNITED STATES PATENT AND TRADEMARK OFFICE

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/939,077 | 08/24/2001 | Garnett , Paul Jeffrey | 5681-03100 | 4242 |

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| EXAMINER |
|---|
| KIM, HONG CHONG |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2186 | 6 |

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| | **Application No.** | **Applicant(s)** |
|---|---|---|
| **Office Action Summary** | 09/939,077 | JEFFREY ET AL. |
| | **Examiner** | **Art Unit** | |
| | Hong C Kim | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>24 August 2001</u>.

2a)☐ This action is **FINAL**.      2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-24</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-24</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>24 August 2001</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All  b)☐ Some *  c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application)
since a specific reference was included in the first sentence of the specification or in an Application Data Sheet.
37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific
reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)      4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)      5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>5</u> .      6) ☐ Other: .

U.S. Patent and Trademark Office

PTOL-326 (Rev. 11-03)      Office Action Summary      Part of Paper No. 6

**Detailed Action**

1.    Claims 1-24 are presented for examination. This office action is in response to the

application filed on 8/24/01.

*Priority*

6.    Receipt is acknowledged of papers submitted on 8/24/01, under 35 U.S.C. § 119, which

papers have been placed of record in the file.

2.    Receipts are acknowledged of information disclosure statement filed on 1/17/02 which

the statement has been placed of record in the file.  Information disclosed and listed on PTO

1449 was considered.

*Specification*

3.    Applicants are requested to include the status of the related U.S. applications, patents, and

foreign application in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in

any other corresponding area in the specification.

4.    The title of the invention is not descriptive.  A new title is required that is clearly

indicative of the invention to which the claims are directed.  The title should be more specific to

differentiate the invention from similar inventions in the patent literature.  The "dirty memory"

and "redundant copies of dirty indicators" aspects of the invention should be mentioned in the

title so that the title is more descriptive.

### *Drawings*

5.    The drawings are objected to because:

Applicant is asked to provide descriptive labels for the black boxes in Fig. 11, Fig.

11A, Fig. 13 Ref. 251, Fig. 14, Fig. 15, Fig. 16 and Fig. 17 to facilitate the general

understanding of the present invention.

6.    Applicants are reminded to maintain clear demarcation to avoid possible double patenting

between US application No. 09/938,800, 09/938,808, 09/939,078, 09/939,277 and the current

application.    Applicants are reminded to maintain a clear line of demarcation between this

application and the pending applications to avoid possible double patenting.

### *Double Patenting*

7.    The non-statutory double patenting rejection, whether of the obviousness-type or non-

obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy

reflected in the statute) so as to prevent the unjustified or improper timewise extension of the

"right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA

1969); *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum,* 686 F.2d 937,

214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8.     Claims 1-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-21 of copending Application No. 09/939,277 in view of Bannon et al. (Bannon) US Patent 5,987,544.

As to claims 1-24, US Application 09/939,277 claims a dirty memory subsystem for a computer system, the dirty memory subsystem comprising storage operable to store dirty indicators, each dirty indicator being associated with a respective block of main memory and being settable to a predetermined state to indicate that the block of main memory associated therewith has been dirtied, However, 09/939,277 does not specifically disclose redundant copies

of dirty indicators.

*Bannon* discloses redundant copies of dirty indicators (abstract) for the purpose of

preventing data loss when one system fail.

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate redundant copies of dirty indicators of Bannon into the

09/939,277 because it would prevent data loss when one system fail.

This is a provisional obviousness-type double patenting rejection because the conflicting

claims have not in fact been patented.


## *Claim Rejections - 35 USC § 102*

9.     The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10.     Claims 1-2, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Bannon et

al. (Bannon) U.S. Patent No. 5,987,544.

As to claim 1, *Bannon* discloses the invention as claimed.  Bannon discloses a dirty

memory subsystem for a computer system, the dirty memory subsystem comprising storage

operable to store redundant copies of dirty indicators (abstract lines 8-11), each dirty indicator

being associated with a respective block of main memory and being settable to a predetermined

state to indicate that the block of main memory associated therewith has been dirtied (col. 2 lines

32-39).

As to claim 2, Bannon discloses the invention as claimed in the above. Bannon further

discloses control logic operable to read the redundant copies of a dirty indicator from storage and

to treat the block of memory associated therewith as dirtied if at least one of the redundant copies

of the dirty indicator has the predetermined state (abstract).

As to claim 12, *Bannon* discloses the invention as claimed. Bannon discloses a computer

system comprising a dirty memory subsystem and at least one processing set that includes main

memory, the dirty memory subsystem comprising storage operable to store redundant copies of

dirty indicators (abstract), each dirty indicator being associated with a respective block of main

memory and being settable to a predetermined state to indicate that the block of main memory

associated therewith has been dirtied (col. 2 lines 32-39).

### *Claim Rejections - 35 USC § 103*

11.    The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth
> in section 102 of this title, if the differences between the subject matter sought to be patented and the prior
> art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12.     Claims 3-10 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Bannon et al. (Bannon) U.S. Patent No. 5,987,544 in view of Garnett U.S. Patent No. 5,991,900.

As to claim 3, Bannon discloses the invention as claimed in the above, however, Bannon

does not specifically disclose the control logic is operable to cause the block of memory

associated with a dirty indicator for which at least one copy thereof has the predetermined state to

be copied from the main memory to another memory.

Garnett discloses the control logic is operable to cause the block of memory associated

with a dirty indicator for which at least one copy thereof has the predetermined state to be copied

from the main memory to another memory (col. 22 lines 32-48) for the purpose of preventing

data loss.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate the control logic is operable to cause the block of memory

associated with a dirty indicator for which at least one copy thereof has the predetermined state to

be copied from the main memory to another memory of Garnett into the invention of Bannon for

the advantages stated above.

As to claim 4, Bannon and Garnett disclose the invention as claimed in the above.

Garnett further discloses the other memory is another main memory (col. 22 lines 33-48).

As to claim 5, Bannon and Garnett disclose the invention as claimed in the above.

Garnett further discloses further discloses operable to reset each of the redundant copies of a

dirty indicator to a state other than the predetermined state after reading the redundant copies of

the dirty indicator (col. 22 lines 26-28).

As to claim 6, Bannon and Garnett disclose the invention as claimed in the above.

Garnett further discloses the storage comprises at least two memory units (col. 22 lines 18+)

each for storing a redundant set of dirty indicators.

As to claim 7, Bannon and Garnett disclose the invention as claimed in the above.

Garnett further discloses the control logic includes comparison logic for each of the memory

units for determining whether a copy of the dirty indicator is set to the predetermined state (col.

22 lines 18+, specifically "The dirty RAM can be reset, or cleared when it is read by a processing

set" reads on this limitation).

As to claim 8, Bannon and Garnett disclose the invention as claimed in the above.

Garnett further discloses the control logic includes output logic responsive to the output of each

comparison logic for determining whether a block of memory associated with a dirty indicator is

to be treated as dirtied (col. 22 lines 18+).

As to claim 9, Bannon and Garnett disclose the invention as claimed in the above.

Garnett further discloses each dirty indicator comprises a single bit (col. 22 lines 18+, bit map).

As to claim 10, Bannon and Garnett discloses the invention as claimed in the above.

Garnett further discloses a block of main memory is a page of main memory (col. 22 lines 18+).

As to claim 13, Bannon and Garnett discloses the invention as claimed in the above.

Garnett further discloses a plurality of processing sets that each include main memory (col. 22 lines 18+).

As to claim 14, Bannon and Garnett discloses the invention as claimed in the above.

Garnett further discloses the processing sets are operable in lockstep, the computer system comprising logic operable to attempt to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error (col. 21 lines 56+).

13.    Claims 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett U.S. Patent No. 5,991,900 in view of Bannon et al. (Bannon) U.S. Patent No. 5,987,544.

As to claim 15, Garnett discloses a method of managing reinstatement of an equivalent memory state in the main memory of a plurality of processing sets of a fault tolerant computer following a lock step error, wherein a dirty memory subsystem stores copies of dirty indicators

that are settable to a predetermined state indicative that a block of main memory associated

therewith has been dirtied, the method including the performance of at least one cycle of copying

any page of main memory that has been dirtied from a first processing set to each other

processing set, each cycle including reading the redundant copies of dirty indicators from storage

and treating a block of memory as dirtied if copy of the dirty indicator has the predetermined

state (col 21 line 55 thru col. 22). However, Garnett does not specifically disclose redundant

copies of dirty indicators.

Bannon discloses redundant copies of dirty indicators (Abstract) for the purpose of

preventing data loss.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate redundant copies of dirty indicators of Bannon into the

invention of Garnett for the advantages stated above.


As to claim 16, Garnett and Bannon disclose the invention as claimed in the above.

Garnett further discloses a block of memory associated with the dirty indicator for which at least

one copy has the predetermined state is copied from the main memory to another memory (col.

22 lines 18+).


As to claim 17, Garnett and Bannon disclose the invention as claimed in the above.

Garnett further discloses the other memory is another main memory (col. 22 lines 18+).

As to claim 18, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses each of the redundant copies of the dirty indicator are reset to a state other than the predetermined state after reading the redundant copies of the dirty indicator (col. 22 lines 18+).

As to claim 19, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses maintaining at least two copies of a dirty indicator in at least two memory units (col. 22 lines 18+).

As to claim 20, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses separately assessing the state of copies of a dirty indicator for each of the memory units for determining whether a dirty indicator is set to the predetermined state (col. 22 lines 18+).

As to claim 21, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses responding to each assessment and determining that the block of memory is dirty if any assessment indicates that the dirty indicator has the predetermined state (col. 22 lines 18+).

As to claim 22, Garnett and Bannon disclose the invention as claimed in the above.
Garnett further discloses each dirty indicator comprises a single bit (col. 22 lines 18+, dirty bit
map).

As to claim 23, Garnett and Bannon disclose the invention as claimed in the above.
Garnett further discloses a block of main memory is a page of main memory (col. 22 lines 18+).

14.     Claim 11 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Bannon et al.
(Bannon) U.S. Patent No. 5,987,544 in view of Watt U.S. Patent No. 6,272,033.

        As to claim 11, Bannon discloses the invention as claimed in the above, however, Bannon
does not specifically disclose a hierarchical dirty memory . Watt discloses a hierarchical dirty
memory (col. 2 lines 12-27) for the purpose of reducing status processing time (col. 2 lines 19-
22).

        Accordingly, it would have been obvious to one having ordinary skill in the art at the time
the invention was made to incorporate a hierarchical dirty memory of Watt into the invention of
Bannon for the advantages stated above.

15.     Claim 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett U.S.
Patent No. 5,991,900 in view of Bannon et al. (Bannon) U.S. Patent No. 5,987,544 and further in
view of Watt U.S. Patent No. 6,272,033.

As to claim 24, Garnett and Bannon discloses the invention as claimed in the above, however, neither Garnett nor Bannon specifically discloses a hierarchical dirty memory . Watt discloses a hierarchical dirty memory (col. 2 lines 12-27) for the purpose of reducing status processing time (col. 2 lines 19-22).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a hierarchical dirty memory of Watt into the combined invention of Garnett and Bannon for the advantages stated above.

## *Conclusion*

16.    The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.    See attached PTO-892.

17.    a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter.  Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

18.    When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the

amendments avoid such references or objections.   See 37 C.F.R. § 1.111(c).


19.     When responding to the office action, Applicants are advised to provide the examiner

with the line numbers and page numbers in the application and/or references cited to assist

examiner to locate the appropriate paragraphs.


20.     Any inquiry concerning this communication or earlier communications from the

Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835.  The

Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

        If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor, Matt Kim, can be reached on (703) 305-3821.

        Any inquiry of a general nature or relating to the status of this application should be

directed to the Group receptionist whose telephone number is (703) 305-3900.


21.         **Any response to this action should be mailed to:**

                Commissioner of Patents and Trademarks
                Washington, D.C. 20231

                **or faxed to TC-2100:**
                Official           (703) 872-9306, New as of 8/4/2003
                After-Final        (703) 746-7238
                Official           (703) 746-7239 (for formal communications intended for
entry)

                Non-Official/Draft (703) 746-7240 (for informal or draft communications, please
label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK

Primary Patent Examiner

November 19, 2003